IN THE CLAIMS

1. (Currently amended): A driver circuit, having at least one input node for an input signal and at least one output node for an output signal, having one or more, preferably two, subdrivers, and having a feedback circuit, which has one or more evaluation circuits and one or more feedback capacitors, the evaluation circuits being connected to the subdrivers and the feedback capacitors respectively being provided between the at least one output node of the driver circuit and an input node of the evaluation circuit, the at least one evaluation circuit having a first inverter stage, coupled to the input node of the evaluation circuit, and a second inverter stage, coupled with the first inverter stage, the first inverter stage comprising at least a first transistor of a first polarity and a first transistor of a second polarity, the second polarity being different from the first polarity, wherein the control terminal of the first transistor of the first polarity and the control terminal of the first transistor of the second polarity are coupled to the input node of the evaluation circuit, wherein a second terminal of the first transistor of the first polarity and a second terminal of the first transistor of the second polarity are coupled to each other and to the input node of the evaluation circuit, wherein the second inverter stage comprises at least a second transistor of the first polarity and a second transistor of the second polarity, and wherein a second terminal of the second transistor of the first polarity and a second terminal of the second

transistor of the second polarity are coupled to each other and to the ~~input node for the input signal~~ subdrivers, wherein a low-harmonics current is generated in the driver circuit and supplied to a load, and wherein an edge steepness that is independent of the present load situation is set in the driver circuit.

2. (Currently amended): The driver circuit as claimed in claim 1, wherein the at least one input node for the input signal [[if]] is connected to the at least one sub-driver.

3. (Canceled)

4. (Previously presented): The driver circuit as claimed in claim 1, wherein at least one subdriver and at least one evaluation circuit is provided, each sub-driver being connected to an evaluation circuit.

5. (Previously presented): The driver circuit is claimed in claim 4, wherein at least one feedback capacitor is provided, each feedback capacitor being provided between the output node of the driver circuit and the input node of an evaluation circuit.

6. (Previously presented): The driver circuit as claimed in claim 1, wherein the input nodes of the evaluation circuits are at low input impedance.

7. (Previously amended): The driver circuit as claimed in claim 1, wherein the at least one sub-driver has one or more transistors.

8. (Previously presented): The driver circuit as claimed in claim 1, wherein at least one control transistor is provided in the at least one sub-driver, said transistor being connected to an evaluation circuit.

9. (Previously presented): The driver circuit as claimed in claim 1, wherein the at least one feedback capacitor is designed as a linear capacitor.

10. (Previously presented): The driver circuit as claimed in claim 1, wherein the at least one feedback capacitor is designed as a nonlinear capacitor.

11. (Previously presented): The driver circuit as claimed in claim 10, wherein the nonlinear capacitor is formed from at least one PMOS transistor and/or at least one NMOS transistor.

12. (Previously presented): The driver circuit as in claim 1 wherein a low-harmonics current is generated in the driver circuit and supplied to a load, and wherein an edge steepness that is independent of the present load situation is set in the driver circuit.

13. (Previously presented): The driver circuit as in claim 12, wherein a $\sin^2$-shaped current is supplied to the load.

14. (Previously presented): The driver circuit as in claim 12 wherein, in order to set the load-independent edge steepness, the output characteristic of the driver circuit is measured by the feedback circuit and evaluated therein, and wherein the driver strength of the at least one sub-driver is regulated on a basis of the evaluation results.

15. (Canceled)

16. (Previously presented): The use of a driver circuit as in claim 1 to improve the electromagnetic compatibility of electronic components, in particular of integrated circuits, wherein a low-harmonics current is generated in the

driver circuit and supplied to a load and wherein an edge steepness that is independent of the present load situation is set in the driver circuit.

17. (Previously presented): The driver circuit as in claim 12 to improve the electromagnetic compatibility of electronic components, in particular of integrated circuits, wherein a $\sin^2$-shaped current is supplied to the load.